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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,699	02/19/2004	Takaaki Negoro	R2180.0190/P190	2014

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EXAMINER
CAO, PHAT X

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EL

Office Action Summary	Application No.	Applicant(s)	
	10/780,699	NEGORO ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *3,4 and 7-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election with traverse of Subspecies 1 claims 1-2, 5 and 6 in the reply filed on 3/8/06 is acknowledged. The traversal is on the ground(s) that the search and examination of an entire application can be made without serious burden on the examiner. This is not found persuasive because Applicant has not provides any reasons to support that the species proposed by the examiner are not distinct species. Furthermore, the search is not coextensive as evidenced by different search for different species. Therefore, the search and examination of the entire application would place a serious burden on the examiner.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Burr (US. 6,121,666).

Regarding claim 1, Burr (Fig. 1C) discloses a semiconductor apparatus including a MOS transistor, the MOS transistor comprising: a semiconductor substrate (232, 234) configured to provide a channel region 244 between a source 236 and drain 238; and a gate electrode 242 formed on the semiconductor substrate via a gate oxide film 240 (column 8, lines 56-57); wherein a threshold voltage of a source side region 236 of the

MOS transistor is higher than that of a drain side region 238 in a longitudinal direction of the channel region (column 3, lines 19-32).

Regarding claim 2, Burr's Fig. 1C also discloses that the threshold voltage of the source side region 236 is designed higher by abutting a pocket region 247 under the source region 236 for differentiating the source and drain side regions in a density of channel impurity in the channel longitudinal direction (column 3, lines 25-33).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr in view of Fisher et al (US. 3, 877,055).

Regarding claim 5, Burr's Fig. 1C does not disclose an addition of an impurity diffusion layer formed between the source and drain as claimed.

However, Fisher (Fig. 10) teaches a MOS transistor comprising: an impurity diffusion layer 33 formed between the source and drain 32 and 34; wherein the channel region is formed from a drain side channel region being formed between the drain 34 and the impurity diffusion layers 33, and the source side channel region being formed between the impurity diffusion layer 33 and the source 32; wherein the gate electrode 53 includes a drain side gate electrode formed on the drain side channel region via a drain side gate oxide film 45, and a source side channel region via a source gate oxide

film 46; wherein the source side region at least includes the source 32, the impurity diffusion layer 33, the source side channel region, the source side gate oxide film 46, and the source side gate electrode 53 so as to collectively form a source side MOS transistor; and wherein the drain side region at least includes the drain 34, the impurity diffusion layer 33, the drain side channel region, the drain side gate oxide film 45, and the drain side gate electrodes 53 so as to collectively from a drain side MOS transistor.

Accordingly, it would have been obvious to modify the MOS transistor of Burr by forming an impurity diffusion layer between the source 236 and the drain 238 because such forming of the impurity diffusion layer would provide a common source-drain for a semiconductor memory device having a fixed threshold MOS device and a variable threshold MOS device, as taught by Fisher et al (column 2, lines 26-31).

Regarding claim 6, Burr (Fig. 1C) further discloses the source and drain side channel regions are different in a density of channel impurity from each other (column 3, lines 25-28).

6. Claims 1-2 and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher et al (US. 3, 877, 055) in view of Burr (US. 6, 121, 666).

Regarding claims 1 and 5, Fisher (Fig. 10) discloses a semiconductor apparatus including a MOS transistor, the MOS transistor comprising: a semiconductor substrate 30 configured to provide a channel region between a source 32 and a drain 34; a gate electrode 53 formed on the semiconductor substrate 30 via a gate oxide film (45,46); and an impurity diffusion layer 33 formed between the source 32 and drain 34; wherein the channel region is formed from a drain side channel region being formed between

the drain 34 and the impurity diffusion layers 33, and the source side channel region being formed between the impurity diffusion layer 33 and the source 32; wherein the gate electrode 53 includes a drain side gate electrode formed on the drain side channel region via a drain side gate oxide film 45, and a source side channel region via a source gate oxide film 46; wherein the source side region at least includes the source 32, the impurity diffusion layer 33, the source side channel region, the source side gate oxide film 46, and the source side gate electrode 53 so as to collectively form a source side MOS transistor; and wherein the drain side region at least includes the drain 34, the impurity diffusion layer 33, the drain side channel region, the drain side gate oxide film 45, and the drain side gate electrodes 53 so as to collectively from a drain side MOS transistor.

Fisher does not disclose that a threshold voltage of a source side region 32 is higher than that of a drain side region 34.

However, Burr (Fig. 1C) teaches a MOS transistor having a threshold voltage of a source side region 236 being higher than that of a drain side region 238 in a longitudinal direction of the channel region 244 by forming a pocket region 247 under the source side region 236. Accordingly, it would have been obvious to form the MOS transistor device of Fisher having a threshold voltage of a source side region 32 being higher than that of a drain side region 34 in order to increase the drive current in the channel region due to the high concentration of mobile charge carriers, as taught by Burr (column 3, lines 37-50).

Regarding claims 2 and 6, Burr's Fig. 1C also teaches that the threshold voltage of the source side region 236 is designed higher by abutting a pocket region under the source region 236 for differentiating the source and drain side regions in a density of channel impurity in the channel longitudinal direction (column 3, lines 25-33).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PC
May 28, 2006

PHAT X. CAO
PRIMARY EXAMINER